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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,865	12/12/2001	Gayvin E. Stong	10011030-1	6882

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EXAMINER
DIMYAN, MAGID Y

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/017,865	Applicant(s) STONG, GAYVIN E.	
	Examiner Magid Y Dimyan	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Dansky et al (henceforth, Dansky) – U.S. Patent No. 6,028,989.

3. Referring to claims 1, 18 and 19, Dansky discloses a computer program and method for noise calculation and modeling that determines crosstalk voltage for a planned chip design by first running routing and crosstalk routines for creating crosstalk rules (see Abstract). Furthermore, the invention cites a direct correlation between noise voltage calculations and transition time degradation for the coupling nets (conductive metal line of the IC). See column 1, lines 55 – 62. Dansky also teaches how to set crosstalk noise limits (i.e., maximum signal transition times) as shown in Fig. 1; Column 1, lines 29 – 54; column 6, line 65 to column 7, line 60, as well as in other portions of the disclosure. Hence, as shown in Fig. 1, potential noise problems (related to transition time degradation) in an IC design can be easily flagged, as claimed herein.

4. As per claims 2, 11 and 20, see (3) above, as well as Tables B and C, and other portions of the disclosure, which cite how the noise analysis is performed based on exact topology and paths of victims and perpetrator nets (i.e., conductor lengths). See also Fig. 2; Table 1, which provide more details of the noise analysis methodology, as claimed herein.

5. As per claims 3, 4, 11and 12, see the Abstract, which cites a program and method that can determine whether a noise problem will potentially occur for a planned IC chip design (i.e., design tool used prior to manufacturing), as claimed herein.

6. As per claims 5, 6, 7 and 14, see (4) above, as well as Fig. 1, which show a) the separate software programs; b) how the information is tabulated (i.e., stored); and c) how the noise analysis is independent of processing technology, as claimed herein.

7. Referring to claims 8, 9, 15 and 16, see Field of Invention (column 1, lines 5 - 10), which cites that this invention pertains to signal coupling between wires used on VLSI Integrated Circuit chips (i.e., MOS/CMOS FET devices).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,389,581 to Muddu et al cites an aspect of interconnect design for optimizing delay characteristics of interconnects, performed by using a method for optimizing repeater positioning at predetermined intervals that are related to signal transition times.

U.S. Patent No. 6,128,769 to Carlson et al discloses a method for analyzing signal noise caused by cross-coupling between an attacker signal line and a victim signal line.

U.S. Patent No. 6,493,853 to Savithi et al teaches a methodology for a practical approach to full chip crosstalk noise verification by forming a multi-dimensional noise lookup table for a cell used within the IC, wherein the noise table relates a set of input noise pulse characteristics and a set of output loading characteristics to the output noise pulse characteristics of the cell.

U.S. Patent No. 6,480,998 to Mukherjee et al relates to a new method of guidance for routing of nets in an IC model wherein all nets are first approximately routed and the victim nets with functional delay noise above predetermined thresholds are identified.

U.S. Patent No 5,568,395 to Huang discloses a system for modeling and estimating crosstalk noise and detecting false logic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (703) 308-1354. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Magid Y Dimyan
Examiner
Art Unit 2825

myd
May 29, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800